Low-Noise Monolithic Ku-Band VCO Using Pseudomorphic HEMT Technology

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***Abstract*—A low-noise pseudomorphic HEMT Ku-band oscillator with varactor frequency tuning and voltage power control is reported. The circuit size, including the varactor and the pads for on-wafer testing, is less than 0.7 mm^2. On-wafer oscillator measurements show a frequency tuning bandwidth of 600 MHz centered at ~15.2 GHz and an output power up to 17 dBm with more than 15 dB of power control. Phase noise of −87 dBc/Hz at 100 kHz has been obtained, which is an excellent result for a fully monolithic integrated Ku-band voltage-controlled oscillator (VCO).**

***Index Terms*— MMIC, phase noise, power control, voltage-controlled oscillator.**

I. Introduction

Low-FREQUENCY (LF) noise is the limiting factor of the close-in to carrier phase noise in solid-state oscillators. The LF noise is upconverted due to nonlinear phenomena and appears as phase noise around the carrier [1]–[3]. Pseudomorphic HEMT technology offers lower LF noise than MESFET and GaAlAs/GaAs HEMT devices [4], which facilitates the achievement of better oscillator phase noise performances. Moreover, heterojunction bipolar transistors (HBT's) have lower LF noise, but because of their greater up-conversion factor [5], this fact does not imply superior oscillator phase noise results compared with pseudomorphic HEMT's.

A low-noise pseudomorphic HEMT monolithic oscillator in the Ku-band with voltage control of frequency and power level is presented. On-wafer oscillator measurements show a frequency tuning bandwidth of about 600 MHz at around 15.2 GHz center frequency and an output power up to 17 dBm with more than 15 dB of power level control. Phase noise of −87 dBc/Hz has been obtained at 100-kHz offset frequency from the carrier. These are excellent results for a fully integrated monolithic Ku-band voltage-controlled oscillator (VCO). The circuit size is less than 0.7 mm^2.

II. Circuit Design

The oscillator has been fabricated using the 0.2-μm pseudomorphic HEMT technology of Philips Microwave Limeil. Recent work [6] gives excellent phase noise results using this technology in a K-band VCO. Fig. 1 shows the circuit photograph. The transistor employed has six fingers of 50 μm. The frequency tuning is achieved with an integrated varactor having four fingers of 50 μm, whose gate length is 3 μm. The circuit topology has been chosen with the aim of having frequency and power tuning possibilities with low phase noise. Wider bandwidth tuning capability is obtained with the varactor connected to the transistor gate as is well known. Nevertheless, we have connected the varactor to the source to minimize the varactor LF noise contribution to the oscillator phase noise, at the expense of frequency tuning bandwidth reduction. Capacitive series feedback and an inductive load connected to the gate have been used in order to obtain negative resistance in the desired frequency range. The load connected to the gate becomes a critical point in the determination of the oscillation frequency. For this reason, the two source terminals are used, one to connect the varactor and the other to bias the transistor, avoiding changes of the gate inductive load when the dc probes and bias cables were connected to the circuit. Two inductors at the drain terminal allow us to set the drain bias and to optimize the load cycle.

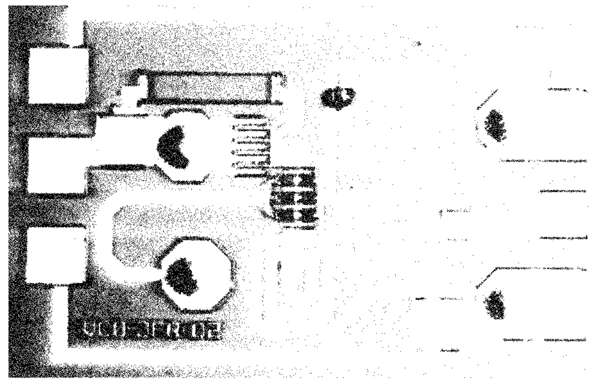

Fig. 1. Photograph of the MMIC oscillator.

Linear and nonlinear analysis techniques have been used at the design stage [7]. Special interest has been taken in the intrinsic load cycle (composition over a period of the intrinsic drain generator instantaneous current and voltage drop) optimization to facilitate the power level control. Phase noise reduction can be achieved by load cycle optimization regarding the bias conditions and the limitation mechanism of the dynamic behavior [8]. Because the noise upconversion factor has a strong dependence on the gate bias [5], the power-level control is performed varying the drain voltage.

Manuscript received July 17, 1997. This work was supported in part by the Spanish “Comisión Interministerial de Ciencia y Tecnología”—CICYT—Reference TIC-93-672-C04-01.

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Publisher Item Identifier S 1051-8207(97)08187-7.

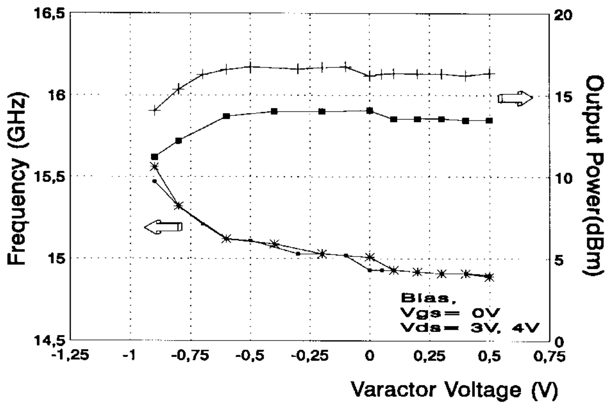

Fig. 2. Measured frequency and power level versus the varactor voltage, for $V_{\rm gs} = 0$ V for various $V_{\rm ds}$.

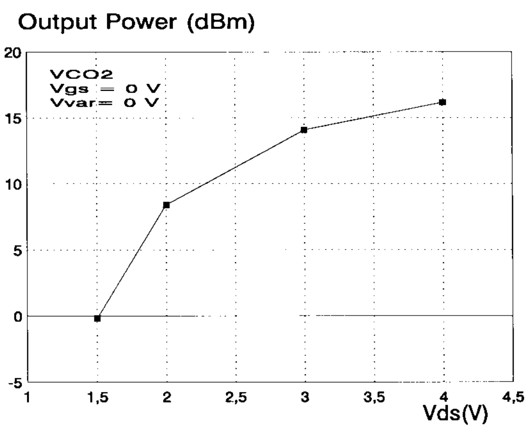

Fig. 3. Measured output power versus the drain bias for null gate bias and varactor voltage.

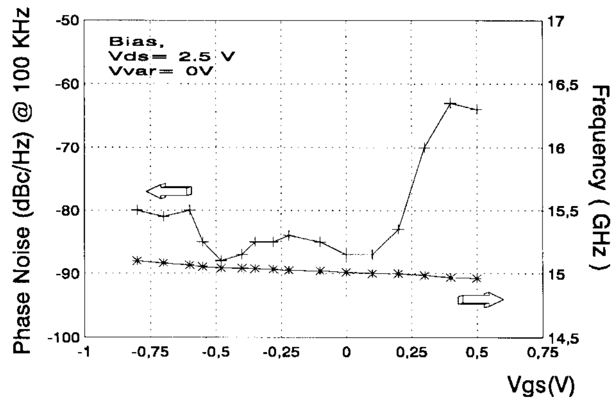

Fig. 4. Phase noise measurements at 100-kHz off-carrier frequency and frequency versus the $V_{\rm gs}$ voltage for drain bias of $V_{\rm ds} = 2.5$ V and null varactor voltage.

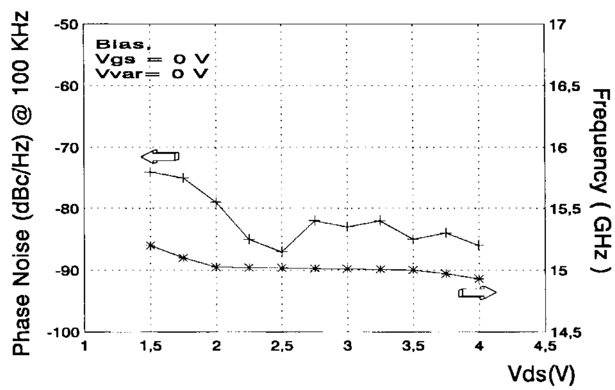

Fig. 5. Phase noise measurements at 100-kHz off-carrier frequency and frequency versus the $V_{\rm ds}$ voltage for gate bias of $V_{\rm gs} = 0$ V and null varactor voltage.

This permits us to obtain more uniform oscillator phase noise performances over the power control voltage range. When the intrinsic load cycle is matched in the nonlinear regime and the transistor bias verifies the maximum power level condition, the load cycle amplitude, and so the power level, can be diminished with the drain bias. In this way, the decreasing drain voltage moves the load cycle toward the ohmic region, limiting the signal excursions and, therefore, the output power.

III. Circuit Performances

On-wafer measurements of frequency tuning, power level control capabilities, and phase noise have been performed using an HP spectrum analyzer. Fig. 2 shows frequency and power versus varactor voltage for gate bias $V_{\rm gs} = 0$ V and $V_{\rm ds}$ as a parameter. Frequency tuning bandwidth is 600 MHz, centered at $\sim$15.2 GHz, with output power up to 17 dBm. Fig. 3 shows the output power versus the drain voltage for null varactor and gate bias voltages. More than 15 dB of power level control is obtained by varying the drain voltage. Figs. 4 and 5 show phase noise measurements versus gate and drain bias conditions, respectively. The associated frequency shifts are also reported. As an example, spectral signal over a 500-kHz frequency span of the oscillator biased at $V_{\rm gs} = 0$ V and $V_{\rm ds} = 2.5$ V is presented in Fig. 6. At particular bias conditions, phase noise of -87 dBc/Hz has been obtained at 100-kHz off-carrier frequency. In Fig. 4, we can see a large increase of phase noise at the highest gate voltages for fixed drain bias. The phase noise also increases at low drain currents but, near pinch-off, measurements have not been performed because of the low oscillation level. For fixed gate bias, we observe in Fig. 5 that phase noise augments as we approach the ohmic region. Nevertheless, differences in phase noise (at 100-kHz off-carrier frequency) less than 5 dBc/Hz are obtained over almost all the drain voltage range of output power control. These phase noise results are excellent for monolithic Ku-band oscillator with varactor frequency tuning and voltage power level control. Certain transistor bias points have been found to be optimum from the point of view of phase noise performances in agreement with other works [5], [9]. The LF noise depends on the nonlinear oscillation regime [9] and the LF noise upconversion is so complex that simple transistor models do not determine accurately the phase noise level. Distributed gate models [10] including the LF noise generators could explain these aspects and aid the design of low-noise oscillators.

IV. Conclusions

A low-noise pseudomorphic HEMT monolithic Ku-band oscillator with varactor frequency tuning and voltage power

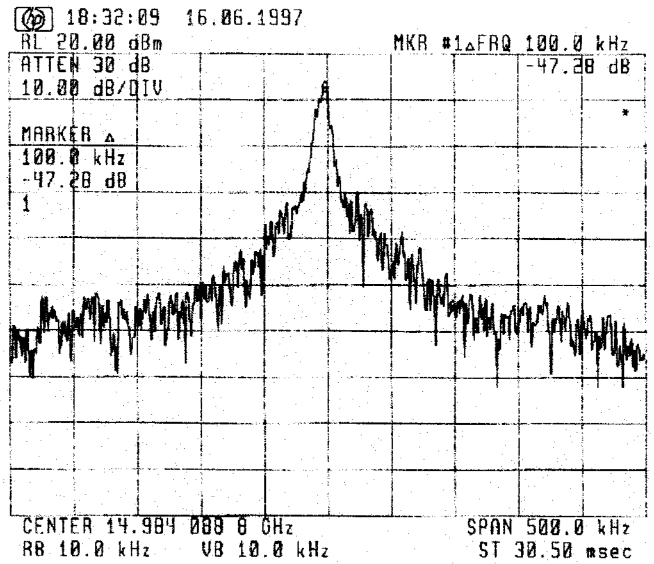

Fig. 6. Oscillator spectrum over a 500-kHz frequency span. Bias conditions are $V_{\rm gs} = 0$ V, $V_{\rm ds} = 2.5$ V, and null varactor voltage.

control has been presented. On-wafer measurements show a frequency tuning bandwidth of about 600 MHz at ∼15.2-GHz center frequency and an output power up to 17 dBm with more than 15 dB of power level control. The phase noise measurements give −87 dBc/Hz at 100-kHz off-carrier frequency. At 100-kHz off-carrier frequency, differences in phase noise of less than 5 dBc/Hz have been obtained over nearly the whole drain voltage range of output power control. These are excellent results for a fully integrated monolithic Ku-band VCO. The circuit size, including the varactor and the pads for on-wafer testing, is less than 0.7 mm^2.

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